KMC PLANAR TRANSISTORS IN MICROWATT LOGIC CIRCUITRY

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INTRODUCTION

This paper will be concerned with the application of a new ultra-high-frequency silicon transistor to logic circuits operating at power levels in the microwatt region.

The device is extremely small and has a base width of about 1/2 micron. It has a maximum frequency of oscillation in excess of one kilomegacycle, while the frequency of unity common emitter current gain is approximately 800 megacycles. The collector capacitance, excluding that of the header, is about 0.6 picofarad.

By means of the planar process,[1] whereby the junction surface is located under oxide, excellent control of surface effects is obtained. The range of usable d-c current gain, h_{FE}, is extended to below one microampere, as shown for a typical unit in Figure 1, because of the reduction in surface recombination. Figure 2 illustrates that the reduction in surface leakage causes a reduction in collector leakage current, I_{CBO}, to values which are far below any operating level, even for microwatt logic.

At the same time, it will be shown that high-speed switching circuits are possible at these low current levels primarily because of the low collector capacity and the high-gain bandwidth product. These will be capable of operating in the 100 kc to 1 mc range at collector currents of from 1 to 10 microamperes, respectively.

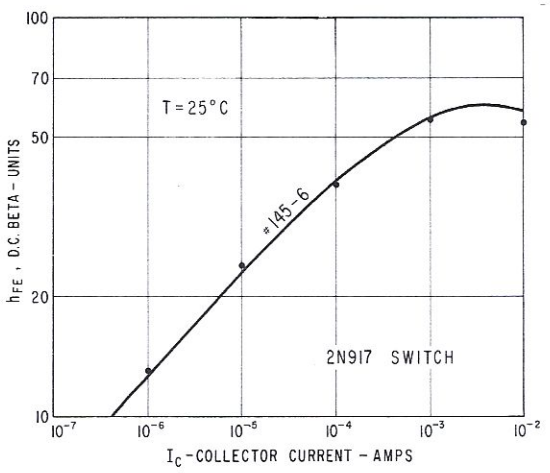

Fig. 1 D-C Current gain for planar transistor extends below 1 μA.

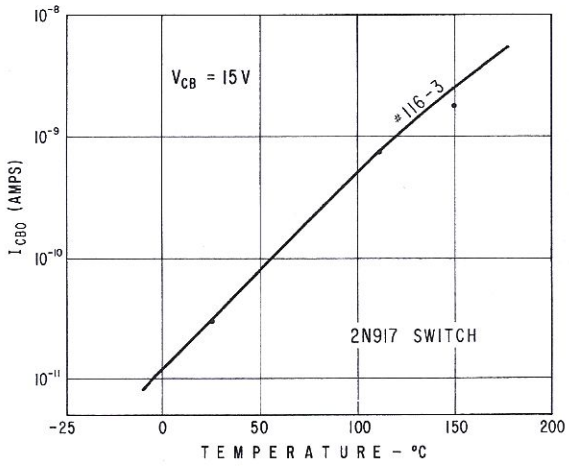

Fig. 2 Planar construction reduces leakage current far below operating level.

BACKWARD DIODE LOGIC

The requirements for lightweight airborne or space equipment has been the major factor for the interest shown in microwatt level circuits. Here the desire for low current drain or low power is augmented by the desirability of simplicity in the logic so as to keep the number of components and therefore the weight to a minimum. Compared to other forms of logic, diode-transistor logic is most desirable from this point of view, because of what might be termed conservation of fan-in or fan-out at a given current level. That is to say that in other forms of logic, such as TRL or DCTL, excess drive current must be supplied to a

given base node to make up for signal "leakage" away from the node. In TRL, the signal leakage is back to other fan-in stages which may be on, and in DCTL the leakage is to other bases in parallel, which "rob" the drive current available to a given base. Thus it may be said that for a given current level per stage, diode transistor logic will give the highest fan-in and fan-out, since there are practically no problems of leakage of available base drive current. If the term "efficiency" may be said to apply to this conservation of fan-in and fan-out at a given current level, then diode-transistor logic may be said to be the most efficient form of transistor logic presently available.

A further simplification of diode logic is offered by the use of backward diodes,[4] such as is shown in the "NOT AND "logic circuit of Figure 3. Here it is seen that there is no need for the voltage translating or compensating devices necessary for turn-off in conventional diode transistor logic. These usually consist of a diode or else a resistor with a parallel capacitor in series with the base with the addition of a negative supply to compensate for the drop through the diode. These components can be eliminated if backward diodes, having much lower drop, are used.

In Figure 3, and henceforth, the terms V_t, or voltage in the tunnelling direction, and V_D, or voltage in the diffusion direction, are used to avoid confusion. The arrow points in the "easy flow" direction.

The "NOR" configuration of Figure 4 is still another possibility, but it may exhibit difficulties of base current robbing, as previously described in connection with DCTL. However, this can be kept to a minimum as long as the collectors are not tied in parallel, which constitutes the worst case condition for this effect in DCTL.

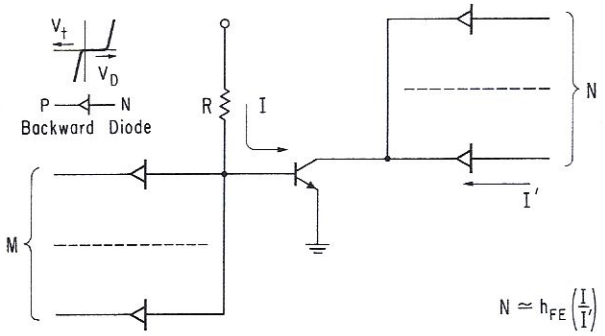

Fig. 3 "NOT AND" logic circuit with backward diodes.

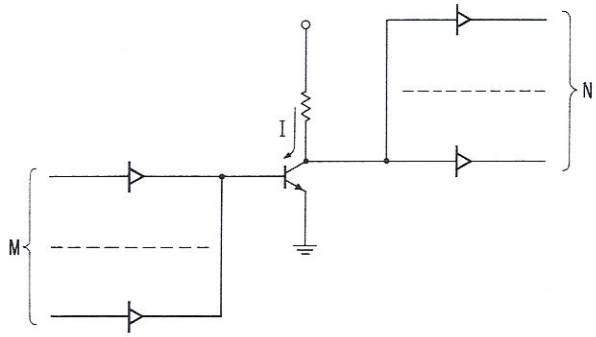

Fig. 4 NOR logic circuit with backward diodes.

DESIGN CONSIDERATIONS

The d-c conditions under which these microwatt circuits will operate is of primary consideration. The formula for fan-out given in Figure 3 is repeated in Appendix I. It shows that fan-out is dependent upon d-c beta and a "current source factor." The current source factor is the ratio of available turn-on base current to collector current which is largely dependent on supply voltage. Therefore, very low voltages can be used when d-c beta is high. However, it will be found that there is a loss of speed below a certain critical voltage. This results from the fact that as voltage is reduced there is a loss in turn-on drive current which causes a deterioration in rise time. For example, the circuits to be described later exhibit a loss in speed below 3 volts, though it would be possible to operate them down to about 1 volt while retaining a fan-out of 3 or 4, if we assume a minimum beta of about 10. This, however, assumes no leakage through

a path such as that of Figure 5. The criterion necessary to keep this leakage to a minimum, shown in the figure, is developed in Appendix II. From this formula it appears that high values of $V_{CE}(sat)$, V_D, and V_t are desirable. This conflicts with the need to keep $V_{CE}(sat)$ and V_t low for turn-off of the following stage, however. A compromise must therefore be made.

Since the changes in $V_{D(TH)}$ and $V_{BE(on)}$ will be in the same direction with temperature, and since V_t changes very little, the change of $V_{CE}(sat)$ with temperature will have the greatest effect on this criterion.

If the above conditions cannot be satisfied, then it would be possible to use two diodes in series in place of one. Alternatively, a saving in diodes can be had by using circuits such as those of Figure 6.

The criterion shown in Figure 5 then becomes that shown in Figure 6A for this configuration. It can be seen that this effectively increases $V_{CE}(sat)$ by adding another V_t term. This formula will be strictly true only if the two diodes are of the same type. It may be advantageous in some cases to increase the size of the drop in the tunnelling direction of diode number 2, and thus greatly increase the effective $V_{CE}(sat)$.

The configuration of Figure 6B effectively raises $V_{CE}(sat)$ by clamping the collector and thus not allowing it to go into saturation. It is shown in Appendix II that in this case the condition of Figure 5 will be satisfied by the first criterion of Figure 6B. This puts the burden of satisfaction of this requirement entirely on the diodes, and should be quite easy to meet. A second restriction is put on the diodes, however; this is necessary to assure turn-off of the following stage. In other words, it must be assured that the resulting effective $V_{CE}(sat)$ is low enough to assure turn-off of the next stage. This is also shown in Appendix III.

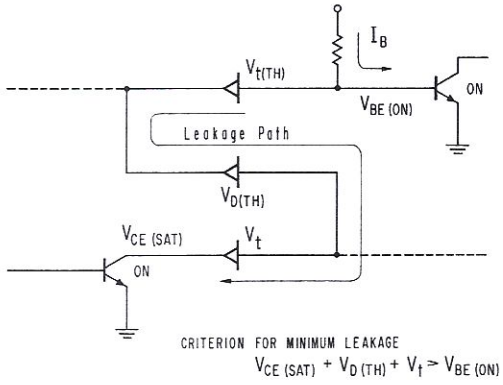

Fig. 5 Criterion for minimum leakage.

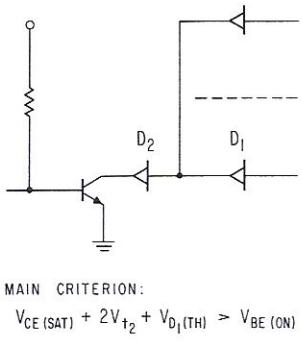

Fig. 6(a) An alternate circuit for Fig.5 which reduces the number of diodes.

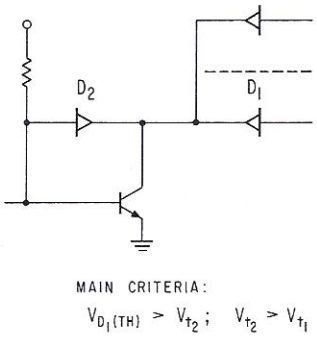

Fig. 6(b) An alternate circuit using a diode clamp on the collector.

To illustrate the characteristics desired in a backward diode for operation at microampere levels, the characteristic curve of an experimental silicon backward diode is shown in Figure 7. These diodes do not display any noticeable negative resistance region as in a tunnel diode. This would actually be detrimental to proper operation of the circuits, since there would be a high value of leakage due to tunnelling current in the diffusion direction. The diodes have been made over a wide range of forward and backward voltage ratio.

RESULTS OF SWITCHING TESTS

Figure 8 shows average propagation time per stage through ten single stages versus current for the DCTL. These are found to be nearly identical. Above about one milliampere, speed is limited by storage; while below about one milliampere, it is limited by fall time. This is due to the long charge-up time of the collector capacitance and associated capacitances to ground through the resistor. Low capacity is, therefore, essential for high speed operation at low currents.[5]

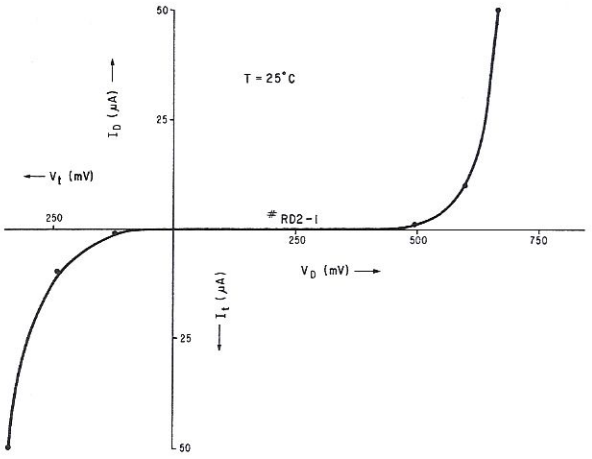

Fig. 7 Desired characteristics of backward diodes for microampere level operation.

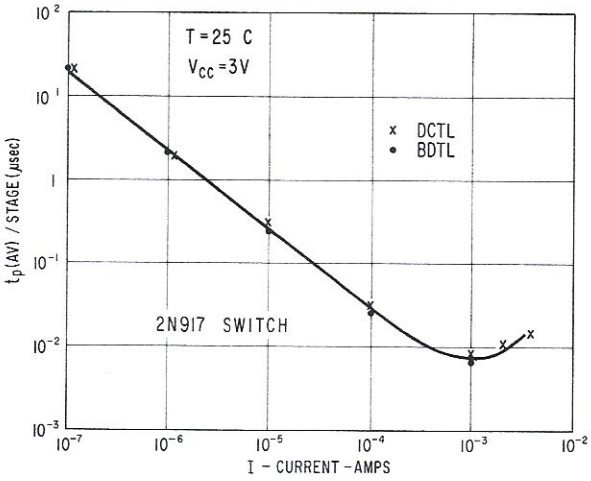

Fig. 8 Average propagation time per stage through ten stages vs. current.

An important point to realize regarding the backward diode logic, as opposed to DCTL, is that this curve represents the worst propagation time at low currents since increased fan-out decreases propagation time. This results because the current available to charge the circuit capacitances is increased with fan-out. This suggests the further possibility that higher level stages would give an increase in propagation time, and this has been found to be the case. In this way, a higher level inverter can be used in a manner similar to the way in which an emitter follower is used to give increased fan-out with little loss of speed, or to step up the current level for going from low to high level operation.

Simulated fan-in had very little effect on speed.

Several flip-flops were built and gave the following results:

Current Level	Switching Rate
100 μA	5 mc
10 μA	1 mc
1 μA	.150 mc

The decrease in switching rate with current is quite noticeable, as should be expected.[6, 7]

TEN MICROAMPERE SHIFT REGISTER

In order to further demonstrate the feasibility of these circuits at low levels, a four-stage shift register of the type shown in Figure 9 was built. This circuit was developed from a basic 10 μA backward diode transistor logic block, from which most of the diodes were eliminated. The resulting circuit is a combination of DCTL and backward diode circuitry; the two are compatible as long as no two bases are connected together.

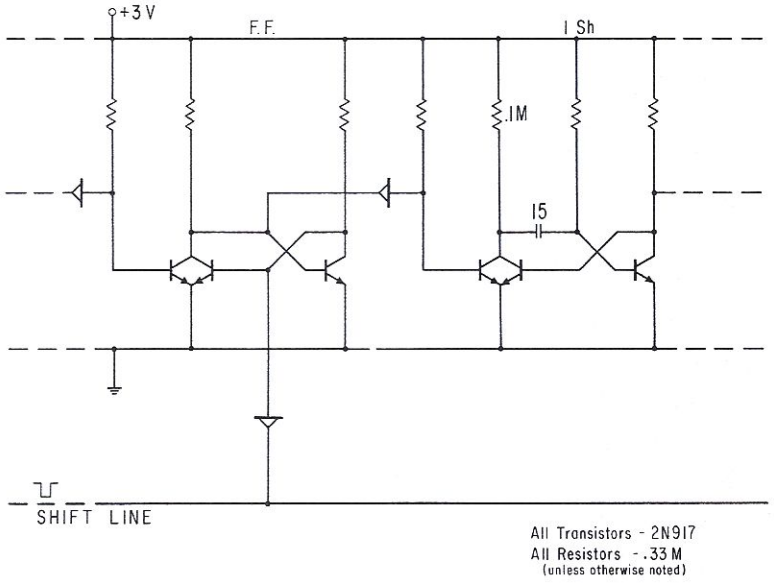

Fig. 9 Four stage shift register that was built using microwatt circuitry.

Operation is such that if a given stage contains a "one" when a reset pulse arrives, it will trigger a one shot which will override the reset pulse on the next stage and thus set it to "one."

This circuit has been found to operate satisfactorily, circulating all possible combinations of one's and zero's, at 200 kilocycles per second over a temperature range of from -49°C to +100°C.

Some difficulty was encountered with feed through of fast signals, since the collector capacitance, diode capacitance, and resistor form a high-pass filter with increasingly lower cutoff frequency as the resistor is increased. However, if the rise time of the driving circuits is kept low, this does not present a problem. Also low capacitance is beneficial in this regard.

There was also considerable trouble with radiated noise pickup, but proper shielding entirely eliminated this problem. The final enclosed circuit is practically impervious to external noise.

The four stage shift register draws about 360 μA of current. A computer using 10,000 transistor building blocks of this type would draw about 100 mA of current, at a power level of 300 mW.

ACKNOWLEDGEMENTS

The authors are indebted to many persons for their help in gathering this material, and would like particularly to thank C. T. Sah for the backward diodes and B. J. Barranger for his work on the circuits.

APPENDIX I

From Figure 3, considering only the collector node, we must require:

$$I h_{FE} = N I' \qquad N = h_{FE}\left(\frac{I}{I'}\right) \tag{1}$$

$$N = h_{fe}\left[\frac{V_{cc} - V_{BE(on)}}{V_{cc} - (V_{CE}(sat) + V_t)}\right] \tag{2}$$

APPENDIX II

Tracing the leakage path of Figure 5, we have: $V_{CE}(sat) + V_t + V_{D(Th)} + V_{t(Th)} > V_{BE(on)}$ (3)

where $V_{D(Th)}$ and $V_{t(Th)}$ are defined as threshold values, specified at a given allowable leakage current. If we assume the worst case, however, $V_{t(Th)}$ might be very small, so that we have approximately:

$$V_{CE}(sat) + V_t + V_{D(Th)} > V_{BE(on)} \qquad V_{BE(on)} - V_{t2} + V_t + V_{D(Th)} > V_{BE(on)} \tag{4}$$

APPENDIX III

In the case of Figure 6B, we have: $V_{CE}(sat) = V_{BE(on)} - V_{t_2}$

Now substituting this into Equation (4): $V_{BE(on)} - V_{t_2} + V_{D_1}(Th) + V_{t_1} > V_{BE(on)}$

$$V_{D_1}(Th) + V_{t_1} > V_{t_2} \tag{5}$$

Therefore, it is adequate to specify: $V_{D_1}(Th) > V_{t_2}$ (6)

For turn off, however, we must specify: $V_{CE}(sat) + V_{t_1} < V_{BE(Th)}$

now substituting for $V_{CE}(sat)$; $\left(V_{BE(on)} - V_{t_2}\right) + V_{t_1} < V_{BE(Th)}$

$$V_{t_2} > V_{t_1} + \left(V_{BE(on)} - V_{BE(Th)}\right) \tag{7}$$

then the least required is: $V_{t_2} > V_{t_1}$ (8)

LIST OF REFERENCES

1. Hoerni, J. A. "Planar Silicon Transistors and Diodes," Presented at 1960 Electron Devices Meeting, Washington, D. C.
2. Cagle, W. B. Chen, W. H. "A New Method of Designing Low Level, High Speed Semiconductor Logic Circuits," 1957 IRE WESCON Convention Record, Part 2.
3. Masher, D. P. "The Design of Diode-Transistor NOR Circuits," IRE Transactions on Electronic Computers, March 1960.
4. Lesk, I. A., et al "Germanium and Silicon Tunnel Diodes - Design, Operation and Application," 1959 IRE WESCON Convention Record, Part 3.
5. Simmons, C. D. "High-Speed Micro-Energy Switching," Solid State Journal, Sept.-Oct. 1960.
6. Suran, J. J. "Speed vs. Circuit Power Dissipation in Flip-Flops," Correspondence, Proc. IRE, Jan. 1959.
7. Suran, J. J. "Circuit Considerations Relating to Microelectronics," Proc. IRE, Feb. 1961.